

$\epsilon_s = 1.03594314\text{e-}10$ (permittivity of silicon)

$q = 1.6021918\text{e-}19$ (electronic charge)

NSUB, PB model parameters

4.23.6 Notes for levels 1, 2 and 3:

The three levels 1 to 3 are as follows:

LEVEL 1	Shichman-Hodges model. The simplest and is similar to the JFET model
LEVEL 2	A complex model which models the device according to an understanding of the device physics
LEVEL 3	Simpler than level 2. Uses a semi-empirical approach i.e. the device equations are partly based on observed effects rather than the theory governing its operation

The L and W parameters perform the same function as the L and W parameters on the device line. If omitted altogether they are set to the option values (set with `.OPTIONS` statement) DEFL and DEFW respectively. These values in turn default to 100 microns.

The above models differ from all other SIMetrix (and SPICE) models in that they contain many geometry relative parameters. The geometry of the device (length, width etc.) is entered on a per component basis and various electrical characteristics are calculated from parameters which are scaled according to those dimensions. This approach is very much geared towards integrated circuit simulation and is inconvenient for discrete devices. If you are modelling a particular device by hand we recommend you use the level 17 model which is designed for discrete vertical devices.

4.23.7 MOS Level 17: Model Parameters

Name	Description	Units	Default
VTO or VT0	Threshold voltage	V	0.0
KP	Transconductance parameter	A/V ²	2.0e-5
GAMMA	Bulk threshold parameter	\sqrt{V}	0.0
PHI	Surface potential	V	0.6
LAMBDA	Channel length modulation	1/V	0.0
RD	Drain ohmic resistance	Ω	0.0
RS	Source ohmic resistance	Ω	0.0
CBD	B-D junction capacitance	F	0.0
CBS	B-S junction capacitance	F	0.0
IS	Bulk junction sat. current	A	1.0e-14
PB	Bulk junction potential	V	0.8
CGSO	Gate-source overlap capacitance	F	0.0
CGBO	Gate-bulk overlap capacitance	F	0.0
CJ	Zero bias bulk junction bottom capacitance	F	0.0
MJ	Bulk junction bottom grading coefficient		0.5
CJSW	Zero bias bulk junction sidewall capacitance	F	0.0

Name	Description	Units	Default
MJSW	Bulk junction sidewall grading coefficient		0.5
FC	Forward bias depletion capacitance coefficient		0.5
TNOM	Parameter measurement temperature	°C	27
KF	Flicker noise coefficient		0.0
AF	Flicker noise exponent		1.0
CGDMAX	Maximum value of gate-drain capacitance	F	0.0
CGDMIN	Minimum value of gate-drain capacitance	F	0.0
XG1CGD	cgd max-min crossover gradient		1.0
XG2CGD	cgd max-min crossover gradient		1.0
VTCDG	cgd max-min crossover threshold voltage	V	0.0
TC1RD	First order temperature coefficient of RD	1/°C	0.0
TC2RD	Second order temperature coefficient of RD	1/°C ²	0.0

4.23.8 Notes for level 17

In SIMetrix version 5.2 and earlier, this model used a level parameter value of 7 instead of the current 17. The number was changed so that a PSpice compatible BSIM3 model (level=7) could be offered. In order to retain backward compatibility, any level 7 model containing the parameters cgdmax, cgdmin, xg1cgd, xg2cgd or vtcdg will automatically be switched to level=17.

The level 17 MOSFET was developed to model discrete vertical MOS transistors rather than the integrated lateral devices that levels 1 to 3 are aimed at. Level 17 is based on level 1 but has the following important additions and changes:

- New parameters to model gate-drain capacitance
- 2 new parameters to model rdson variation with temperature.
- All parameters are absolute rather than geometry relative. (e.g. capacitance is specified in farads not farads/meter)

All MOSFET models supplied with SIMetrix are level 17 types. Many models supplied by manufacturers are subcircuits made up from a level 1, 2 or 3 device with additional circuitry to correctly model the gate-drain capacitance. While the latter approach can be reasonably accurate it tends to be slow because of its complexity.

Gate-drain capacitance equation:

$$C_{gd} = \left(0.5 - \frac{1}{\pi} \tan^{-1} ((VTCDG - v) - XG1CGD) \right) CGDMIN \\ + \left(0.5 - \frac{1}{\pi} \tan^{-1} ((VTCDG - v) XG2CGD) \right) CGDMAX$$

where v is the gate-drain voltage. This is an empirical formula devised to fit measured characteristics. Despite this it has been found to follow actual measured capacitance to remarkable accuracy.

To model gate-drain capacitance quickly and to acceptable accuracy set the five C_{gd} parameters as follows:

1. Set CGDMIN to minimum possible value of C_{gd} i.e. when device is off and drain voltage at maximum.
2. Set CGDMAX to maximum value of C_{gd} i.e. when device is on with drain-source voltage low and gate-source voltage high. If this value is not known use twice the value of C_{gd} for $V_{gd} = 0$.
3. Set XG2CGD to 0.5, XG1CGD to 0.1 and leave VTCGD at default of 0.

Although the parasitic reverse diode is modelled, it is connected inside the terminal resistances, RD and RS which does not represent real devices very well. Further, parameters such as transit time (TT) which model the reverse recovery characteristics of the parasitic diode are not included. For this reason it is recommended that the reverse diode is modelled as an external component. Models supplied with SIMetrix are subcircuits which include this external diode.

4.24 BSIM3 MOSFETs

4.24.1 Notes

The BSIM3 model is available with *Pro* and *Elite* versions. versions of SIMetrix. Three versions are supplied namely 3.1, 3.24 and 3.3. Our implementation of version 3.1 includes all bug fixes applied to the latest version but the device equations and supported parameters are for the original version 3.1. See below to find out how to switch versions.

BSIM3 models can be accessed using one of four values for the LEVEL parameter:

LEVEL=7 specifies a PSpice compatible model

LEVEL=8 specifies the standard Berkeley BSIM3 model.

LEVEL=49 specifies the Hspice® implementation using the Hspice® junction capacitance model.

LEVEL=53 is also a Hspice® version but uses the standard Berkeley junction cap model.

The following PSpice parameters are supported when using level 7: TT, L, W, RG, RD, RS, RB, RDS, JSSW

The following Hspice® parameters are supported when using level 49/53: CJGATE, HDIF, LDIF, WMLT, XL, XW, IS, N, NDS, VNDS, PHP, LMLT, CTA, CTP, PTA, PTP, TREF, RD, RS, RDC, RSC, CBD, CBS, FC, TT, LD, WD, EG, GAP1, GAP2, XLREF, XWREF, ACM, CALCACM, TLEV, TLEVC

The Hspice® noise model is also supported for NLEV=0,1 and 2.

The 'M' instance parameter has also been implemented with all variants. This specifies the number of equivalent parallel devices.

Additional temperature parameters: All variants support the TEMP and DTEMP instance parameters. TEMP specifies absolute temperature (Celsius) while DTEMP specifies the temperature relative to the circuit global temperature.

All variants support the model parameters T_MEASURED (equivalent to TNOM), T_ABS (as TEMP instance parameter) and T_REL_GLOBAL (as DTEMP instance parameter)

4.24.2 Version Selector

The VERSION parameter can be specified to select which version is used. As detailed above, SIMetrix supports three different BSIM3 versions although 8 versions have been released by Berke-